--Although modifications and changes may be suggested by those skilled in the art, it is the intention of the inventors to embody within the patent warranted hereon all changes and modifications as reasonably and properly come within the scope of their contribution to the art.--

At page 12, line 1, change "Patent Claims" to --WHAT IS CLAIMED IS:--.

IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) A [Computer] computer-supported method for partitioning an electrical circuit comprising the steps of:[,]

- [whereby] imaging the electrical circuit is imaged onto a graph that exhibits the same topology as the electrical circuit[,];

- [whereby] allocating weighting values to edges of the graph [have weighting values allocated to them] with which a required calculating outlay for determining electrical descriptive quantities for elements of the electrical circuit that are represented by the respective edge is described[,];

- [whereby] a first sum value of the weighting values of the edges [is calculated] for edges coupled to one another and, in further iterations, the first sum value is respectively formed upon addition of at least one further edge until the respectively calculated, first sum value is greater than a [prescribable] prescribable, first threshold[,];

- [whereby] forming a partition of the electrical circuit [is formed] by the edges taken into consideration in the formation of the first sum value[,];

- [whereby the following steps are implemented] for at least a part of the remaining edges that do not lie in the partition and that are coupled to at least one edge of the partition[:];

- determining a second sum value [is determined] that derives from the sum of the first sum value and at least one weighting value of at least one remaining edge[,];

- when the second sum value is smaller than a prescribable second threshold, and [-- ]when a plurality of edges that were taken into consideration in the formation of the second sum value that are coupled to edges that were not taken into consideration in the formation of the second sum value is smaller than a plurality of edges of the partition that are coupled to the remaining edges, then

- allocating the remaining edge [is allocated] to the partition and allocating the second sum value [is allocated] to the first sum value, and

- [whereby] forming the partition [is formed] by the edges taken into consideration in the formation of the second sum value.

2. (Amended) [Method] The method according to claim 1, [whereby a] wherein, at the beginning of the method, grouping of elements of the electrical circuit for which it is respectively found that these elements are allocated in common to a partition [is implemented at the beginning of the method].

Acted

3. (Amended) [Method] The method according to claim 2, [whereby] wherein at least one of the following rules is applied in the grouping of the elements of the electrical circuit:

- elements of a controlled source, at least a controlling element and the controlled source, are allocated in common to a partition,

- connecting loops in the electrical circuit that only contain at least one voltage source and at least one counter-inductance are allocated in common to a partition,

- no shorts dare arise due to the partitioning.

4. (Amended) [Method] The method according to [one of the claims 1 through 3, whereby] claim 1, wherein a plurality of edges of the graph have a common weighting value allocated to them.

5. (Amended) [Method] The method according to [one of the claims 1 through 4, whereby] claim 1, wherein the graph of the partition is imaged onto the electrical circuit, whereby the partition comprises the elements of the electrical circuit corresponding to the implemented partitioning.

6. (Amended) [Method] The method according to [one of the claims 1 through 5] claim 1, comprising the further steps of:

- [whereby] iterating the method a plurality of times thereby forming a plurality of partitions [are formed by multiple implementation of the method], and

- [whereby the] determining electrical descriptive quantities for the elements of the electrical circuit [are determined] for each partition, [whereby] at least a part of the partitions [is] being processed in parallel on the plurality of computers and/or processors.

7. (Amended) [Method] The method according to claim 6, [whereby] wherein the parallel processing of the partitions is centrally controlled.

8. (Amended) [Method] The method according to claim 7, [whereby] wherein at least a part of the partitions are centrally controlled in such a way that all terminals of the respective partition are coupled only to a central control unit and[, thus,] a communication of data ensues only between the central control unit and at least the part of the partitions.

9. (Amended) [Method] The method according to claim 8, [whereby] a voltage source is additionally allocated at least to a part of the terminals of the respective partition, the value of said additional voltage source [to be] predetermined by the central control unit during the determination of the electrical descriptive quantities.

10. (Amended) [Method] The method according to claim 9, [whereby] wherein a resistor is additionally allocated at least to a part of the terminals of the respective partition.

IN THE ABSTRACT OF THE DISCLOSURE

At page 15, line 1, change "ABSTRACT" to --ABSTRACT OF THE DISCLOSURE--.

At page 15, line 2, delete "Computer-Supported Method for Partitioning an Electrical Circuit".

Please amend the Abstract of the Disclosure to read as follows:

A partition of an electrical circuit is formed in that the electrical circuit is imaged on a graph (102) and weighting values are allocated (103) to the edges of the graph. The weighting values describe a required calculating outlay for determining electrical descriptive quantities for the respective element of the electrical circuit represented by the edge. A check